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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,286	12/03/2003	Gary S. Ditlow	BUR920030122US1	1285

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EXAMINER
SIEK, VUTHE

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,286	DITLOW ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12,14-19,21-25,27-32,34 and 35* is/are rejected.

7)☒ Claim(s) *6,13,20,26 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/3/03;2/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/707,286 filed on 12/3/2003.

Claims 1-35 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 7, 15-19, 21-25, 27-32 and 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Igusa et al. (6,249,902).

4. As to claims 1, 21, 28 and 35, Igusa et al. teach a method of partitioning an integrated circuit (IC) design comprising identifying logical blocks within said IC design (Figs. 3A-F, and its description); eliminating overlapping logical blocks that overlap above an overlap percentage limit (col. 5, lines 52-67; Fig. 5A-B; 6A-B; 7, and its description); and expanding remaining logical blocks to cover unused space within boundaries of said IC design (Fig. 5A-B, 6A-B and its description).

5. As to claims 2, 22 and 29, Igusa et al. teach identifying primary logical blocks comprising the highest level of logical design hierarchy of said IC design; for each ones of said primary logical blocks that have a size above a predetermined maximum size limit, identifying secondary logical blocks of the second-highest level of said logical design hierarchy; and iteratively repeating said process of identifying secondary logical

blocks for additional levels of said logical design hierarchy until all logical blocks are within the predetermined maximum size limit (Fig. 3A-B, 4, 14; col. 5, lines 12-35).

6. As to claims 3, 23 and 30, Igusa et al. teach the circuit design is recursively horizontally and vertically partitioned until the average number of cells partitioned in each section is less than a defined threshold value (col. 5, 61-67; col. 7-10).

7. As to claims 4, 24 and 31, Igusa et al. teach identifying primary logical blocks comprising the highest level of logical design hierarchy of said IC design; and for ones of said primary logical blocks that have a size below a predetermined minimum size limit, combining said primary logical blocks until a combination of said primary logical blocks exceeds said predetermined minimum size limit (col. 5).

8. As to claims 5, 25 and 32, Igusa et al. teach the circuit design is recursively horizontally and vertically partitioned until the average number of cells partitioned in each section is less than a defined threshold value (col. 5, 60-67; col. 7-10).

9. As to claims 7, 27 and 34, Igusa et al. teach expanding sides of the remaining blocks until said sides reach another block or reach a boundary of said IC design; formation additional rectangles from remaining unused space; and incorporating said additional rectangles into adjacent blocks (Fig. 5A-B and its description; 14-A-D; 15A-D).

10. As to claim 15, remarks set forth in rejection claim 1 apply. In addition, Igusa et al. teach expanding sides of the remaining blocks until the sides reach another block or reach a boundary of the IC design; forming additional rectangles from the remaining

unused space; and incorporating the additional rectangles into adjacent blocks (Fig. 14-15).

11. As to claim 16, remarks set forth in rejecting claim 2 apply because of similar claimed limitations.

12. As to claim 17, remarks set forth in rejecting claim 3 apply because of similar claimed limitations.

13. As to claim 18, remarks set forth in rejecting claim 4 apply because of similar claimed limitations.

14. As to claim 19, remarks set forth in rejecting claim 5 apply because of similar claimed limitations.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 8-12 and 14 are rejected under 35 U.S.C. 103(a) as being obvious over Igusa et al. (6,249,902) in view of Boyle et al. (6,557,145).

17. As to claim 8, remarks set forth in claim 1 equally apply in rejecting claim 8. Igusa et al. teach the logic blocks are within a predetermined maximum size limit (at least each partitioning level, an initial seed partition of the logic modules within an area to be partition is selected in a way to keep intact as many modules of the highest

possible level of the logic hierarchy; col. 5) and a predetermined minimum size limit (the circuit design is recursively horizontally and vertically partitioned until the average number of cells partitioned in each section is less than a defined threshold values (col. 5); partitioning said integrated circuit design into partitions corresponding to said remaining blocks (Fig. 3). Igusa et al. do not teach running applications within each partition of said integrated circuit design in parallel. Boyle et al. teach that a parallel processing system suitable for implementing a concurrent design optimizer on each partition in order to achieve high performance (see summary; col. 8 line 10 to col. 9 line 14; Fig. 4). Combining these teachings would have been obvious to one of ordinary skill in the art at the time the invention was made in order to obtain high performance as expected.

18. As to claim 9, remarks set forth in rejecting claim 2 apply because of similar claimed limitations.

19. As to claim 10, remarks set forth in rejecting claim 3 apply because of similar claimed limitations.

20. As to claim 11, remarks set forth in rejecting claim 4 apply because of similar claimed limitations.

21. As to claim 12, remarks set forth in rejecting claim 5 apply because of similar claimed limitations.

22. As to claim 14, remarks set forth in rejecting claim 7 apply because of similar claimed limitations.

Allowable Subject Matter

23. Claims 6, 13, 20, 26 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach or fairly suggest the process of eliminating overlapping logical blocks comprising initially eliminating overlapping blocks based on the overlap percentage limit; counting the total number of remaining blocks; and revising said overlap percentage limit if the total number of remaining blocks is outside the range of the desired number of logical blocks.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER